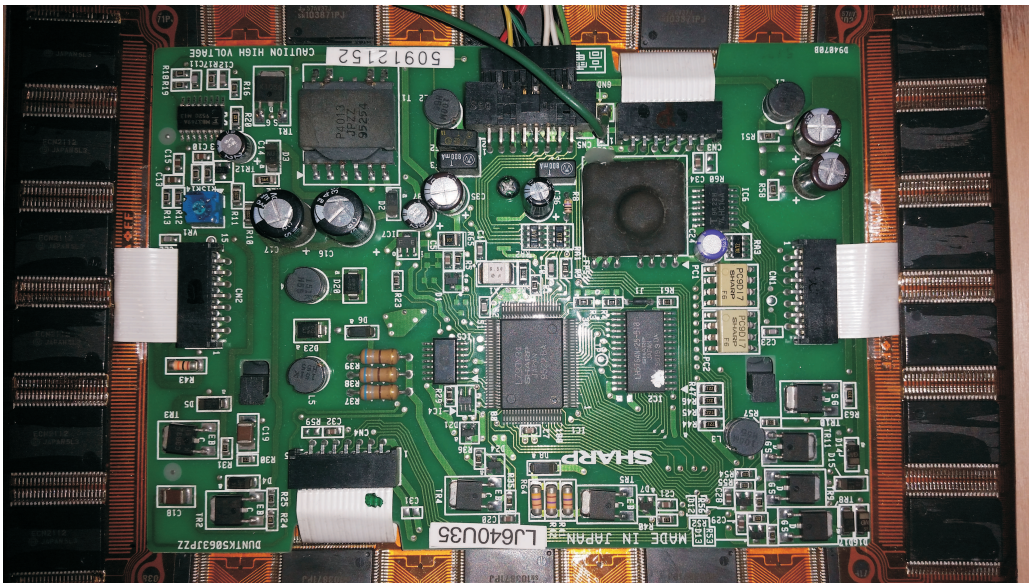
SHARP

LJ640U35

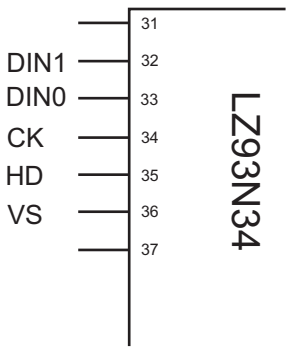
640 x 400 EI Display Module

or any other EL/Plasma display based on LZ93N34 chip,
product specifications.



Input connector: 16 pin 0.1” (8x2) angle connector.

Pin No.	signal name	description, value
1	nc	no connection
2	nc	
3	Vcc	+5V, power for logic chips
4	Vcc	+5V
5	Vee	+12V plasma power suply
6	Vee	+12V
7	GND	ground
8	GND	
9	CK	pixel clock
10	nc/GND	
11	VD	vertical synchro
12	GND	
13	HD	horizontal synchro
14	GND	
15	D0	display data, column odd
16	D1	display data, column even



LJ640U35, 640 x 400 El Display Module by SHARP.

Input signals timing characteristics (Ta=25°C)

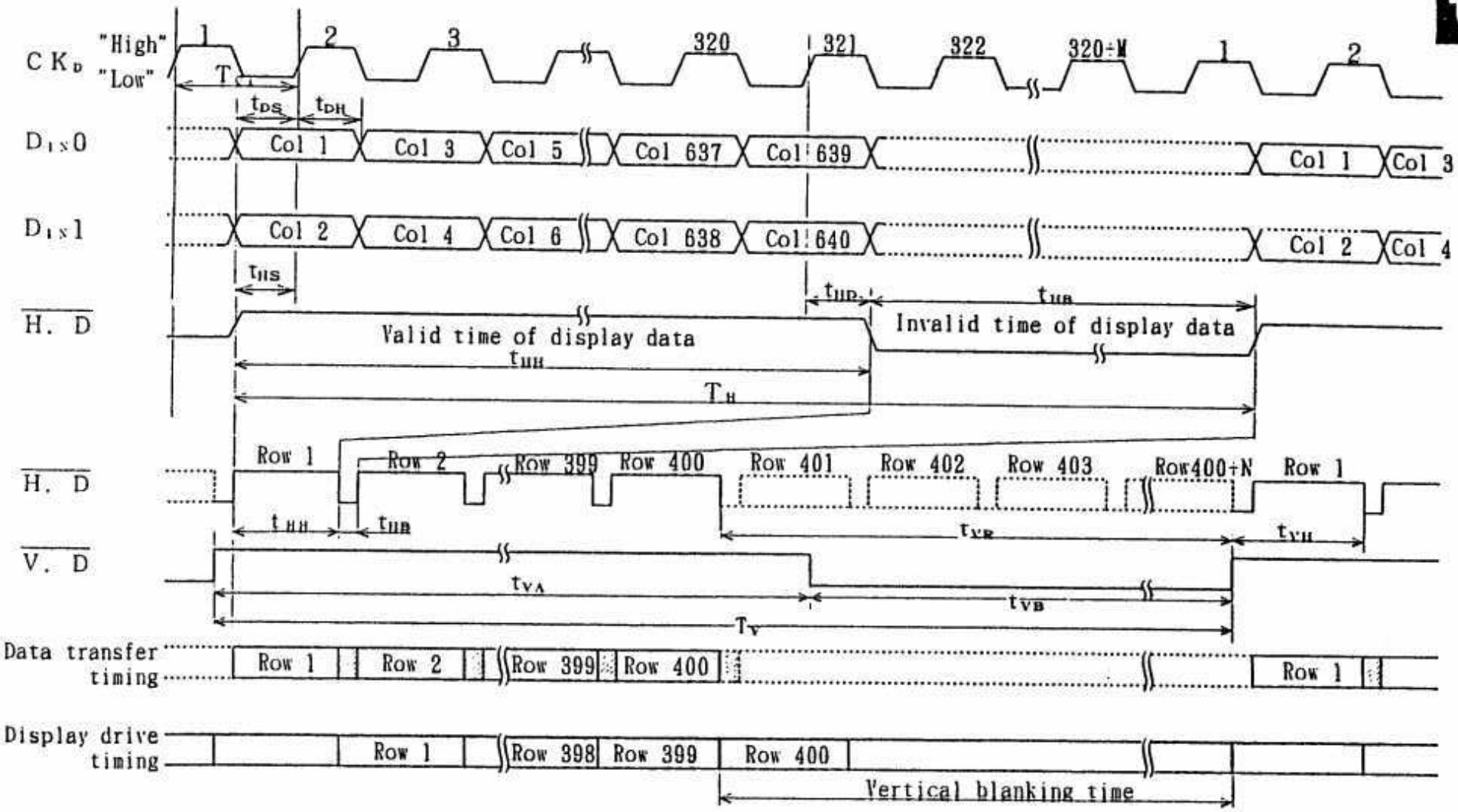
Parameter	symbol	Min.	Typ.	Max.	Unit.
Clock frequency	1/Tcl	7.5	-	11.5	MHz
Clock duty	Tcl(II)/Tcl * 100	45	-	55	%
Horizontal sync. signal cycle time	th	40	-	45	µs
Horizontal sync. signal blanking time	thb	2	-	-	µs
Vertical sync. signal blanking time	tvb	1	-	N x th	µs
Vertical sync. signal valid time	tva	400xth	-	-	µs
Frame Frequency	1/tv	55	60	62	Hz
Data signal set up time	tds	20	-		ns
Data signal hold time	tdh	20	-		ns
Horizontal sync. signal set up time	ths	20		tcl/2	ns
Horizontal sync. signal hold time	thd	20		tcl/2	ns
Vertical sync. signal rise wait time	tvr	4x40	-	-	µs
Vertical sync. rise timing	tvh	40	-	th-tws+35 *	µs

*-note. Unreadable original chip datsheet data.
General note: screen is still working at lower frequencies, but flickering.

THIS IS PLASMA DISPLAY PANEL, do not keep static image for a long time- burn out is very possible.
Display color: amber

8. Timing Chart

Interface Timing and Display drive timing



Note 1) Logic level is not necessary to be specified in dotted line portion.

Note 2) $t_{HB} \geq 2$ μs shall be kept. ($t_{HH} = M \times T_{CL}$)

Note 3) $N \geq 4$ shall be kept.